

WHAT IS CLAIMED IS:

1 1. An integrated circuit incorporating an Electrostatic Discharge (ESD)
2 protection device comprising:
3 a semiconductor substrate;
4 an electrical contact pad;
5 an ESD switch coupled to the pad and having an active device region
6 formed in the semiconductor substrate; and
7 a dynamic shock absorbing region formed in the semiconductor
8 substrate adjacent to said active device region, said dynamic shock absorbing
9 region made from a material with thermo-mechanical properties substantially
10 more resistant to shock from dynamic effects of ESD than said active device
11 region.

1 2. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said thermo-
3 mechanical properties include a dynamic loss factor higher than
4 approximately 0.01.

1 3. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said thermo-
3 mechanical properties further include a melting temperature higher than
4 approximately 800 °K.

1 4. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said thermo-
3 mechanical properties further include a moderately low stiffness as defined by
4 an elastic modulus approximately in the range of 10 GPa and 100 GPa (Giga
5 Pascals).

1 5. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said thermo-
3 mechanical properties further include a tensile strength higher than
4 approximately 100 MPa.

1 6. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein the ESD switch has
3 one or more sides, and wherein the dynamic shock absorbing region formed
4 in the semiconductor substrate is located in trenches adjacent to the one or
5 more sides of the ESD switch.

1 7. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein the ESD switch is a
3 transistor.

1 8. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein the dynamic shock
3 absorbing region is configured above the active device region.

1 9. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein the dynamic shock
3 absorbing region is configured below the active device region of the ESD
4 switch.

1 10. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said dynamic shock
3 absorbing region made from a material with thermo-mechanical properties
4 substantially more resistant to dynamic shock than said active device region is
5 selected from the group consisting of hard polymers, amorphous carbon,
6 carbon-carbon composite or carbon-polymer composite.

1 11. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 1, wherein said dynamic shock
3 absorbing region is surrounded by a dielectric region.

1 12. An integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device comprising:
3 a semiconductor substrate;
4 an ESD switch having an active device region formed in the
5 semiconductor substrate; and
6 a plurality of dynamic shock absorbing regions formed around the
7 active device region, said dynamic shock absorbing region made from a
8 material with thermo-mechanical properties substantially more resistant to
9 shock from dynamic effects of ESD than said active device region.

1 13. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein said thermo-
3 mechanical properties include a dynamic loss factor higher than
4 approximately 0.01.

1 14. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein said thermo-
3 mechanical properties further include a melting temperature higher than
4 approximately 800 °K.

1 15. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein said thermo-
3 mechanical properties further include a moderately low stiffness as defined by
4 an elastic modulus approximately in the range of 10 GPa and 100 GPa (Giga
5 Pascals).

1 16. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein said thermo-
3 mechanical properties further include a moderately high tensile strength
4 higher than approximately 100 MPa.

1 17. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, further comprising a dielectric
3 layer formed in between said ESD switch and said dynamic shock absorbing
4 region.

1 18. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12 and further comprising a
3 passivation layer formed above said dynamic shock absorbing region.

1 19. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein said ESD switch has a
3 gate region and wherein said gate region is formed from a thermo-mechanical
4 energy sink material, said thermo-mechanical energy sink material
5 substantially more resistant to thermo-mechanical expansion than the
6 semiconductor substrate.

1 20. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 19, wherein said thermo-
3 mechanical energy sink material has physical properties including a high
4 melting temperature higher than approximately 2000 °K.

1 21. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 19, wherein said thermo-
3 mechanical energy sink material has physical properties further including a
4 high tensile strength higher than approximately 300 MPa.

1 22. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 19, wherein said thermo-
3 mechanical energy sink material has physical properties further including a
4 low thermal expansion coefficient lower than approximately $5 \times 10^{-6} \text{ }^{\circ}\text{K}^{-1}$.

1 23. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, further comprising a second
3 dynamic shock absorbing region formed in the semiconductor substrate in
4 thermal contact with said active device region, said second dynamic shock
5 absorbing region made from a material with thermo-mechanical properties
6 substantially more resistant to shock from the dynamic effects of ESD than
7 said active device region.

1 24. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 12, wherein the ESD switch has
3 one or more sides, the device further comprising a third dynamic shock
4 absorbing region located adjacent to the one or more sides of the ESD switch.

1 25. An integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device comprising:
3 a semiconductor substrate;
4 an ESD circuit comprising a switch having an active device region
5 formed in the semiconductor substrate and one or more passive circuit
6 components; and
7 means for absorbing dynamic shock from at least one of the switch and
8 one or more passive components in response to an ESD event.

1 26. An integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 25, wherein said means for
3 absorbing shock comprises a region above the active device region made
4 from a material with thermo-mechanical properties resistant to shock from

5 dynamic effects of ESD, the thermo-mechanical properties including a high
6 material dynamic loss factor higher than approximately 0.01.

1 27. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 25, and further comprising a
3 second dynamic shock absorbing region formed below the active device
4 region, said second dynamic shock absorbing region made from a material
5 with thermo-mechanical properties resistant to shock from the dynamic effects
6 of ESD, the thermo-mechanical properties including a high material dynamic
7 loss factor higher than approximately 0.01.

1 28. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 25, wherein the ESD switch also
3 has one or more sides, wherein the means for absorbing shock further
4 comprises a third dynamic shock absorbing region formed adjacent to the one
5 or more sides of the ESD switch, said third dynamic shock absorbing region
6 made from a material with thermo-mechanical properties resistant to shock
7 from the dynamic effects of ESD, the thermo-mechanical properties including
8 a high material dynamic loss factor higher than approximately 0.01.

1 29. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 25, wherein said ESD switch has a
3 gate region and wherein said gate region is formed from a thermo-mechanical
4 energy sink material, said thermo-mechanical energy sink material
5 substantially resistant to thermo-mechanical expansion and having physical
6 properties including a low thermal expansion coefficient lower than
7 approximately $5 \times 10^{-6} \text{ }^{\circ}\text{K}^{-1}$.

1 30. The integrated circuit incorporating an Electrostatic Discharge
2 (ESD) protection device according to claim 25, wherein said active device
3 region is formed from a thermo-mechanical energy sink material, said thermo-
4 mechanical energy sink material substantially resistant to thermo-mechanical

5 expansion and having physical properties including a low thermal expansion
6 coefficient lower than approximately $5 \times 10^{-6} \text{ }^{\circ}\text{K}^{-1}$.

1 31. A method of fabricating an ESD device on a semiconductor
2 substrate, the method comprising:
3 fabricating a switch from connectors and active device regions formed
4 in the semiconductor substrate;
5 providing a dynamic shock absorbing region formed in the
6 semiconductor substrate adjacent said active device regions, said dynamic
7 shock absorbing region made from a material with thermo-mechanical
8 properties substantially resistant to shock from dynamic effects of ESD.

1 32. A method of fabricating an ESD device on a semiconductor
2 substrate according to claim 31, wherein said thermo-mechanical properties
3 including a high material dynamic loss factor higher than approximately 0.01.

1 33. The method of fabricating an ESD device on a semiconductor
2 substrate according to claim 31 wherein said thermo-mechanical properties
3 further include a moderate melting temperature material higher than
4 approximately 800 °K.

1 34. The method of fabricating an ESD device on a semiconductor
2 substrate according to claim 31, wherein said thermo-mechanical properties
3 further include a moderately low stiffness as defined by an elastic modulus
4 approximately in the range of 10 GPa to 100 GPa (Giga Pascals).

1 35. The method of fabricating an ESD device on a semiconductor
2 substrate according to claim 31, wherein said thermo-mechanical properties
3 further include a moderately high tensile strength higher than approximately
4 100 MPa.